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LOW LEAKAGE CHARGE RECYCLING TECHNIQUE FOR POWER MINIMIZATION IN CNTFET CIRCUITS

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Abstract. Carbon Nanotube Field Effect Transistor (CNTFET) is one of the most promising candidates in the near future for digital design due to its better electrostatics and higher mobility characteristics. Parameters that determine the CNTFET performance are the number of tubes, pitch, diameter and oxide thickness. In this paper, a power gating design methodology to realise low power CNTFET digital circuits even under device parameter changes is presented. Investigation about the effect of different CNTFET parameters on dynamic and standby power is carried out. Simulation results reveal that the power gated circuits suppress a maximum of about 67 % dynamic power and 59 % standby power compared to conventional circuits.

Keywords: Carbon Nanotube Field Effect Transistor (CNTFET); power gating; power dissipation; leakage; dynamic power.

1. Introduction

Power dissipation has become an important reliability issue in the design of submicron level digital devices. Current CMOS technology encounters considerable challenges like short-channel effects, lack of control over leakage and source-to drain tunnelling [1–6]. CNTFETs are considered as a promising alternative to the CMOS technology in future nanometre digital design. CNTFETs have many advantageous characteristics like high electron mobility, large current carrying capability and smaller device footprint compared to MOSFETs [7]. In recent years, attempts on modelling and simulating CNTFETs [8, 9] are made for estimating their performance at the device level. The main idea of the paper is to reduce the power dissipation of CNTFET digital circuits by using a methodology called power gating.

In this paper, a low leakage charge recycling (LLCR) powergating technique designed for CMOS circuits has been tested with CNTFET digital circuits like an inverter, multiplexer, VCO, and SRAM cell for a low power dissipation. A power estimation is done for these digital circuits with and without the LLCR technique.

The paper is organized as follows: Section 2 briefs about the structure and equivalent circuit of the CNTFET, and power gating techniques. Section 3 presents the proposed LLCR power gating technique and its functionality. Simulation results are analysed in section 4 and section 5 concludes the work.

2. Literature review

2.1. Power gating techiques

The power gating approach cuts off the power to the circuit blocks when they are not in use [10, 11]. The transistor-based power gating is implemented by placing sleep transistors in-line between the circuit and the power network or the ground network. Mutoh et al. [12] proposed a power gating technique in which the circuit blocks operate in active and sleep modes. Sleep mode offers high leakage reduction, but the data in circuit blocks are lost. This becomes undesirable if the standby duration is short. To preserve the data in the circuit block during idle periods, an intermediate data retention mode is required.

Many power gating approaches [13–16] have been proposed for data retention with an intermediate power saving mode (drowsy mode) wherein a significant voltage difference is maintained across the circuit blocks by boosting the virtual ground voltage. Clamping devices like diodes and transistors are used for raising the virtual ground voltage. Sleepy keeper approach [13] uses additional transistors between the circuit output and supply rails to retain the data in drowsy mode. This approach is not emphatically used to dynamically change the output voltage but instead only used to maintain an already calculated output voltage. Dual diode Vth approach [14] utilizes diodes in parallel with sleep transistors for the data retention. Sleep mode is lost in this technique and hence it is not suitable when the circuit remains idle for long periods. The dual switch approach [15] employs transistors in parallel with sleep transistors for drowsy mode. Dual diode switch approach [16] uses a series combination of diode and transistor, in parallel with sleep transistors for data storage in idle periods. Area overhead of dual switch and dual diode Vth approach is high because of additional diodes and transistors. In these techniques [13–16], the charge gets stored at the gate of the sleep transistor during active mode, and it is dumped to ground and wasted during mode transitions. No attempt is made to reuse the charge.

S. No	Powergating Techniques	Modes of Operation	Data Retention	Charge Recycling
1	Sleep Approach	Two	No	No
2	Sleepy Keeper Approach	Two	Yes	No
3	Dual diode Vth Approach	Two	Yes	No
4	Dual switch approach	Three	Yes	No
5	Dual diode switch Approach	Three	Yes	No
6	Sleep Buffer Approach	Two	Yes	Yes
7	Trimodal Switch Approach	Three	Yes	Yes
8	Charge Recycling Approach	Three	Yes	Yes
9	Low Leakage Charge Recycling (LLCR) Approach (Proposed)	Three	Yes	Yes

TABLE 1. Comparison between other power gating techniques and proposed LLCR technique.

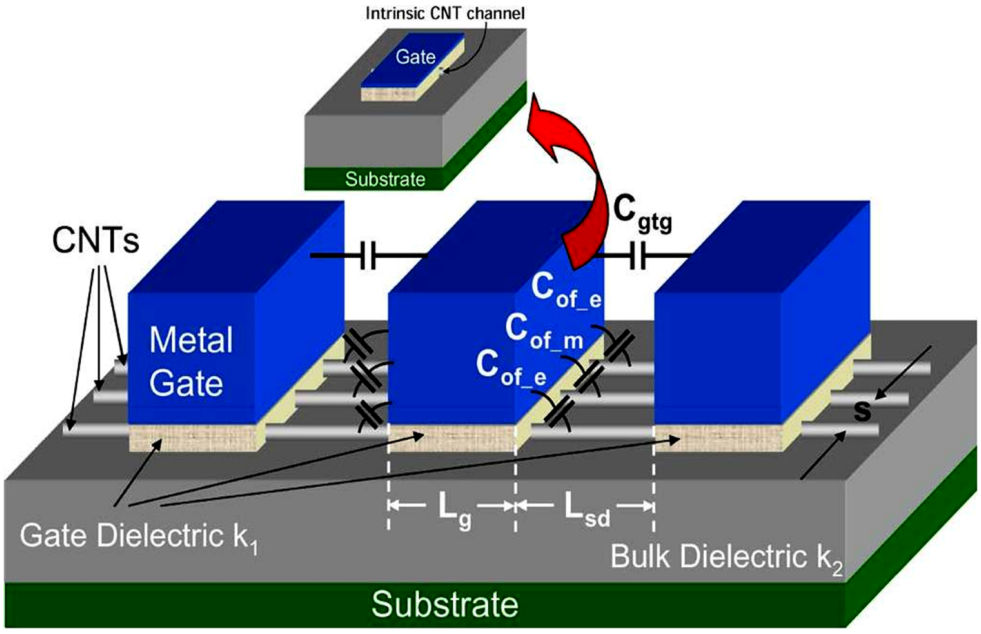

FIGURE 1. Three-dimensional device structure of CNTFETs [8].

The sleep buffer approach [17] increases the virtual ground voltage by reusing the charge at the gate of the sleep transistor without using clamping devices. Data is retained in this technique and it works well when the circuit switches between active and drowsy modes frequently. But the leakage is high when circuit is idle for long duration as there is no sleep mode in this technique. The trimodal switch approach [18, 19] also utilizes the charge recycling concept and offers active, sleep and drowsy modes, but it is not efficient in terms of area. A sneak path exists in trimodal switch approach from the supply to the ground through the sleep and drowsy transistors which increases the leakage. The charge recycling technique [20] reuses the charge at the gate of the sleep transistor with the help of a pass transistor during mode transitions but the leakage power is soaring. In this paper, an efficient low leakage charge recycling (LLCR) power gating technique is proposed, which offers three modes of operation, less area and high power reduction based on charge recycling concept. Table 1 presents the comparison between the conventional power gating methods and the proposed LLCR technique.

2.2. CARBON NANOTUBES

The CNTFET has four terminals similar to the traditional silicon MOSFET device. Figure 1 shows the three-dimensional device structure of CNTFETs with multiple channels and related parasitic gate capacitances. In Figure 1, three CNTFETs are fabricated along one single carbon nanotube (CNT). Undoped semiconducting nanotubes are placed under the gate as channel region and heavily doped CNT segments are placed between the gate and the source/drain to allow low series resistance in the ON-state [21–24]. The device is electrostatically turned 'on' or 'off' by controlling the gate potential. The threshold voltage of the CNT channel varies in accordance with chirality and diameter.

An equivalent circuit model for the channel region of a basic CNTFET is shown in Figure 2. The current sources modelled in the equivalent circuit are be-

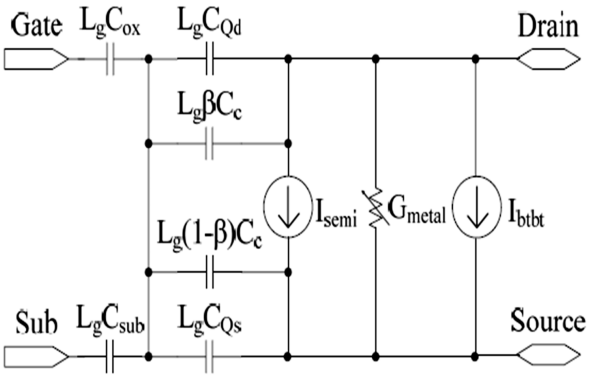

Figure 2. Six-capacitor equivalent circuit model for the intrinsic channel region of CNTFET [8].

cause of: (i) the semiconducting sub-bands thermionic current (I_{semi}); (ii) the metallic sub-bands current ($_{Imetal}$); and (iii) the band to band tunnelling (BTBT) leakage current (I_{btbt}) [8]. The thermionic current of the semi conducting sub-bands is given by

$$I_{\text{semi}(\text{V}_{\text{ch,DS}},\text{V}_{\text{ch,GS}})} = \frac{4e^2}{h}\sum_{m=1}^{M} T_m\left(V_{\text{ch,DS}} + \frac{kT}{e}\ln\frac{1+e^{\frac{E_{m,0}-\Delta\phi_{\text{B}}}{kT}}}{1+e^{\frac{E_{m,0}-\Delta\phi_{\text{B}}+eV_{\text{ch,DS}}}{kT}}}\right) \quad (1)$$

where, $\Delta\Phi_{\text{B}}$ is the channel surface potential charge, $V_{\text{ch,DS}}$ and $V_{\text{ch,GS}}$ are the Fermi potential differences within the channel, M is the number of sub-bands, e is the unit electronic charge, $E_{m,0}$ is the half band gap of the mth sub-band, T is the temperature in Kelvins, T_m is the transmission probability and k is the Boltzmann constant.

A voltage controlled current source Ibtbt in the device model is to evaluate the device sub-threshold behaviour and the static power dissipation [8]. Band-to-band tunnelling (BTBT) current turns out to be a significant component in the sub-threshold region. Assuming a ballistic transport for the tunnelling process, the band-to-band tunnelling current is approximately given by the BTBT tunnelling probability (Tbtbt) times the maximum possible tunnelling current integrating from the conduction band at the drain side up to the valance band at the source side.

$$I_{\text{btbt}} = \frac{4e}{h}kT\sum_{m=1}^{M} T_{\text{btbt}}\ln\frac{1+e^{\frac{eV_{\text{ch,DS}}-E_{m,0}-E_{\text{f}}}{kT}}}{1+e^{\frac{E_{m,0}-E_{\text{f}}}{kT}}} \times \frac{\max\{eV_{\text{ch,DS}}-2E_{m,0},0\}}{eV_{\text{ch,DS}}-2E_{m,0}}, \quad (2)$$

where T_{btbt} is the Wentzel–Kramers–Brillouinlike transmission coefficient and E_{f} is the Fermi level of the doped source/drain in electron-volt units. In metallic nanotubes, the sub-band current comprises both the hole and electron currents [8]. The equation for I_{metal}

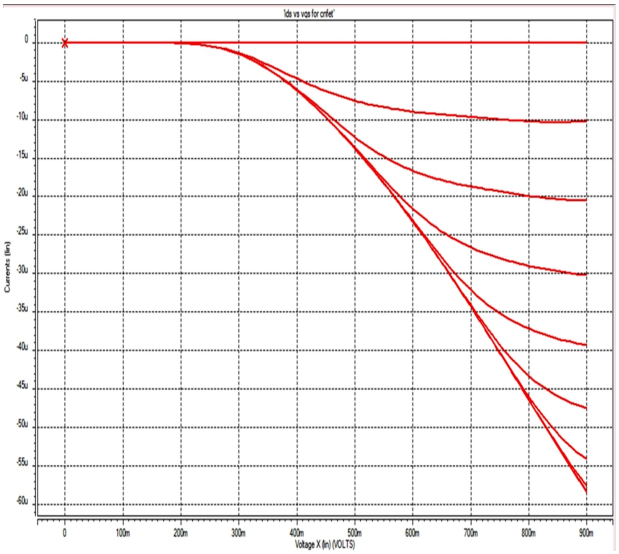

Figure 3. V–I characteristics of N-CNTFET.

can be expressed as

$$I_{\text{metal}} = (1-m_0)\frac{4e^2}{h}T_{\text{metal}}V_{\text{ch,DS}}, \quad (3)$$

where T_{metal} is the transmission probability and m_0 is the zeroth sub-band reserved for the metallic sub-band. Equation (3) confirms that I_{metal} does not depend upon the surface-potential change $\Delta\Phi_{\text{B}}$ and it depends only on $V_{\text{ch,DS}}$ and T_{metal}.

3. LLCR power gating structure

Figures 3 and 4 show the simulated voltage (V_{gs})–current (I_{ds}) characteristics of the CNTFETs. It is clear that the V–I characteristics of the CNTFETs are similar to those of MOSFET [6] and hence the power gating structure proposed for MOSFET digital circuits can also be extended to carbon nanotubes. As an attempt, the low leakage charge recycling (LLCR) power gating technique shown in Figure 5 is used for minimizing the power dissipation in CNTFET digital circuits.

The LLCR technique enables three different circuit operation modes: active, sleep and drowsy depending on the values of the control signals as shown in Table 2. In this work, only active (dynamic) and sleep (static) power minimization is given an importance. Dynamic power is the power consumed when the circuit block is in active state and static power is the power dissipated when the circuit has no input transitions [25–29]. A P-CNTFET transistor (PST) at the supply rail and N-CNTFET transistor (NST) at the ground rail are the sleep transistors and they are used for the power gating. The drowsy transistor (MD) is to support the data retention mode (drowsy mode).

Sleep Mode. In the standby mode, transistors PST, NST and MD are "off". The circuit blocks are disconnected from the supply and ground rails. The voltage across circuit block is zero and it enters into deep sleep

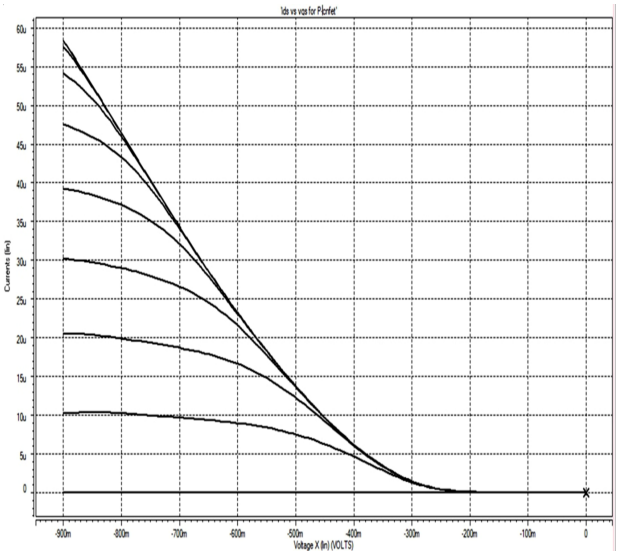

FIGURE 4. V–I characteristics of P-CNTFET.

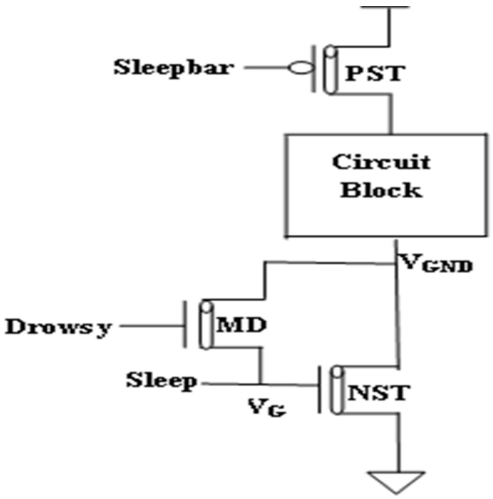

FIGURE 5. Low Leakage Charge Recycling (LLCR) technique with CNTFET.

Sleep	Sleep bar	Drowsy	Circuit Mode
1	0	0	Active
0	1	0	Sleep
0	0	1	Drowsy

TABLE 2. LLCR technique functionality.

mode. The leakage power of digital circuits is high, if it is in direct contact with V_{DD} due to the tunnelling of more electrons. In digital circuits without a power gating, the entire transistors in the pull up network are connected to V_{DD}, which means that there are higher possibilities of electrons tunnelling from the gate to the source [30]. But in the LLCR technique, only the sleep transistor (PST) is in a direct contact with V_{DD} and all other transistors in the pull up network are connected through the PST thus the leakage power is drastically reduced compared to conventional circuits.

D0	D1	Select	Select Bar
0	0	0	1
0	1	0	1
1	0	0	1
1	1	0	1
0	0	1	0
0	1	1	0
1	0	1	0
1	1	1	0

TABLE 3. Input sets for a 2 : 1 multiplexer static power measurement.

Active Mode. In the active mode, the transistor PST is "on" and MD is "off". The virtual ground (V_{GND}) voltage is approximately at zero level. As the *sleep* signal level rises, the voltage at the gate of the NST transistor (V_{G}) is increased and the electric charge gets stored at V_{G} and NST is "on".

The circuit blocks are connected with the supply rails and the effective supply voltage experienced by the circuit block is (V_{DD}–V_{thp}–V_{thn}), where V_{thp} and V_{thn} are the threshold voltages of PST and NST respectively. If digital circuits across the circuit blocks are not power gated, the voltage level experienced by the circuit blocks is V_{DD}. As the net voltage across the circuit block is lessened by the threshold voltage of the sleep transistors, the dynamic power is highly alleviated in powergated circuits compared to conventional digital circuits.

Drowsy Mode. The drowsy mode is meant for the data retention in circuit blocks and it is not considered in this paper. Data is retained by raising the virtual ground voltage and maintaining a significant voltage across the blocks. In the LLCR technique, during the drowsy mode, the transistor MD is "on". The charge stored at the gate of the NST transistor (V_{G}) during the active mode increases the virtual ground voltage (V_{GND}) through the MD. This process continues until the charges at the V_{GND} and V_{G} are equalized, and the V_{GND} voltage reaches an equilibrium (V_{cr}) at the balance point of the leak current of the circuit block and the current through the sleep transistor. Thus, the voltage level of the VGND node is increased to V_{cr} and the voltage across the circuit block is (V_{DD}–$|V_{\mathrm{tp}}|$–V_{cr}), which is sufficient to retain the data in the circuit blocks. In digital circuits without power gating, there is no possibility for the data retention.

4. Simulation results

For evaluating the performance of the LLCR power gating structure, it is applied to inverter, 2 : 1 multiplexer, voltage controlled oscillator (VCO) and static random access memory (SRAM), as these are the basic circuits for a digital circuit design. Synopsys HSPICE and 32 nm Stanford CNTFET models [32] are used for carrying out the circuit simulation. 0.9 V supply

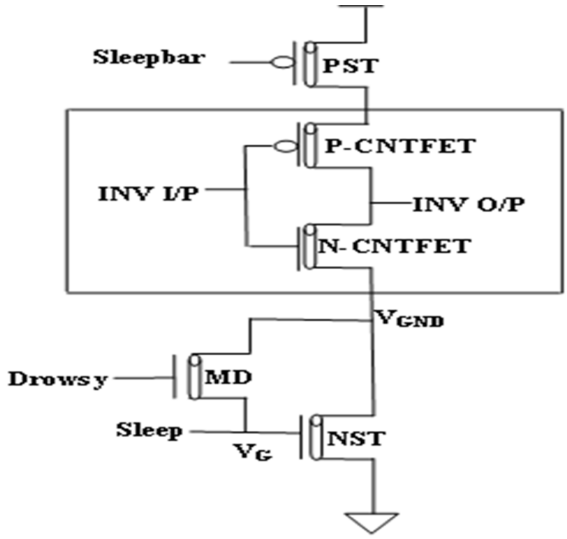

Figure 6. Integration of inverter within LLCR.

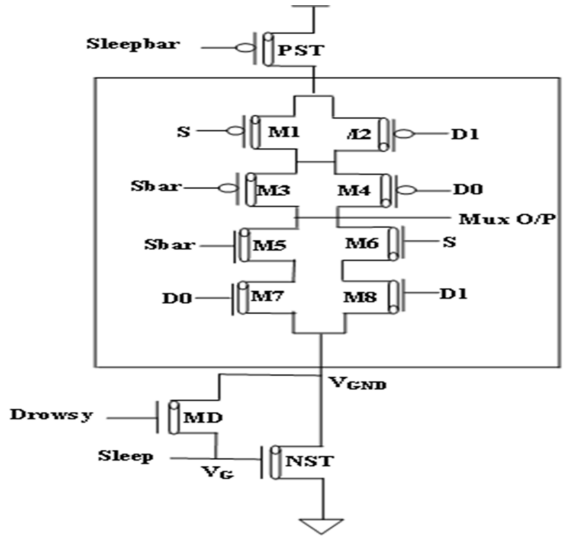

Figure 7. Integration of 2 : 1 multiplexer within LLCR.

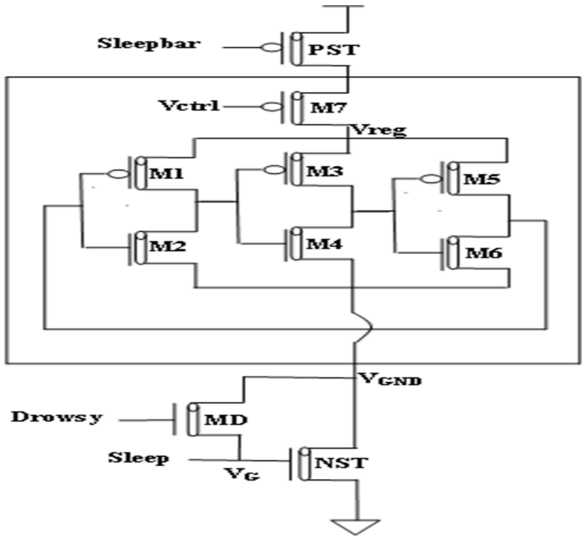

Figure 8. Integration of VCO within LLCR.

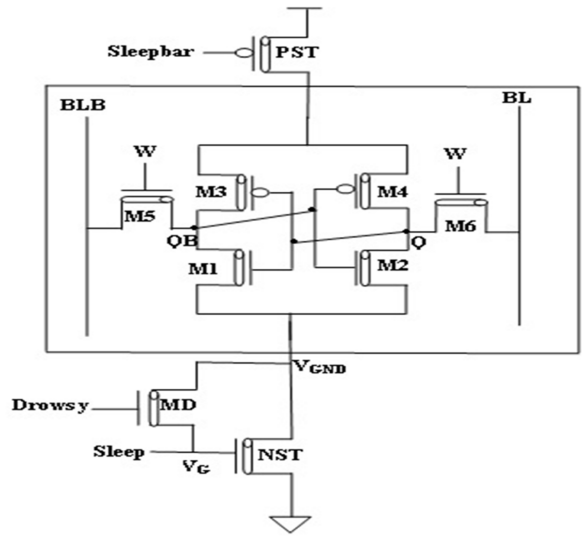

Figure 9. Integration of SRAM Cell within LLCR.

voltage and 27 °C temperature are considered for the experimentation of digital circuits. Power dissipation is estimated with and without the power gating structure for the above mentioned circuits, by varying the CNTFET device parameters like CNTFET diameter (D_{CNT}), number of carbon nanotubes (N), pitch distance (S) and oxide thickness (T_{ox}). This is done to assess the effect of these device parameters on power.

A subset of possible input combinations is considered to estimate the static power as leakage power varies according to the input state. Eight random input vectors shown in Table 3 are considered for the 2 : 1 multiplexer out of 16 possible input combinations. Two input vectors 1 and 0 are considered for the inverter. The SRAM cell is held in the hold mode for the leakage power measurement. When an input vector is asserted, the power dissipation is measured after the signal becomes stable (e.g., after 50 ns). The leakage power of each circuit is derived by averaging the power dissipation for all input combinations.

The dynamic power is estimated by asserting semi-random input signals. Inputs are chosen so that a large number of possible input combinations are included in the set. The average power dissipation reported by the HSPICE is taken as the estimate of the dynamic power dissipation. The active power of the inverter is measured by asserting a pulse signal with a frequency of 10 MHz. For the SRAM cell, the inputs are chosen so that the cell is maintained both in read and write mode in alternate clock cycles. For a 2 : 1 multiplexer, the input vectors are chosen to represent a sample of possible inputs, with at least two of the four input bits at every clock cycle change. A circuit implementation of the VCO consists of an odd number of inverting stages and its working is controlled by the voltage applied to it. For a simulation of the VCO, 0.9 V control voltage is applied and a power estimation is done. Figures 6–9 show the integration of inverter, 2 : 1 multiplexer, VCO and SRAM cell within the LLCR respectively.

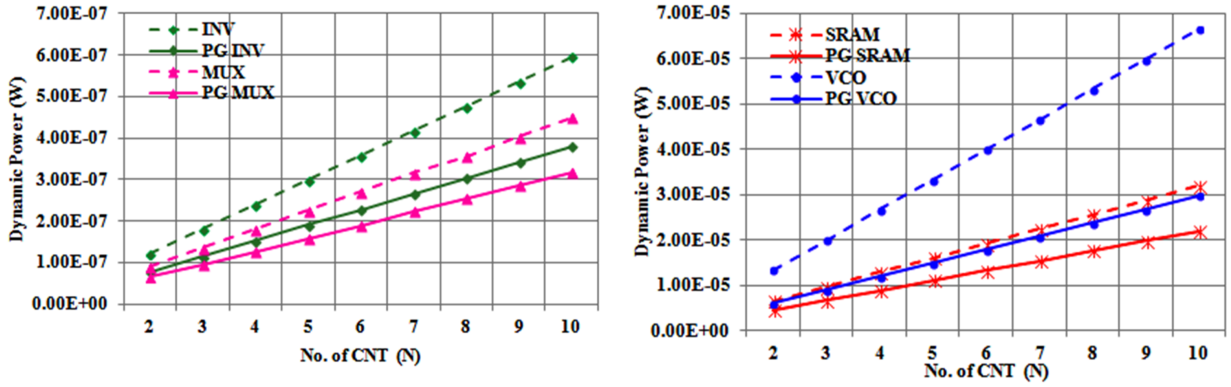

FIGURE 10. Effect of N on dynamic power.

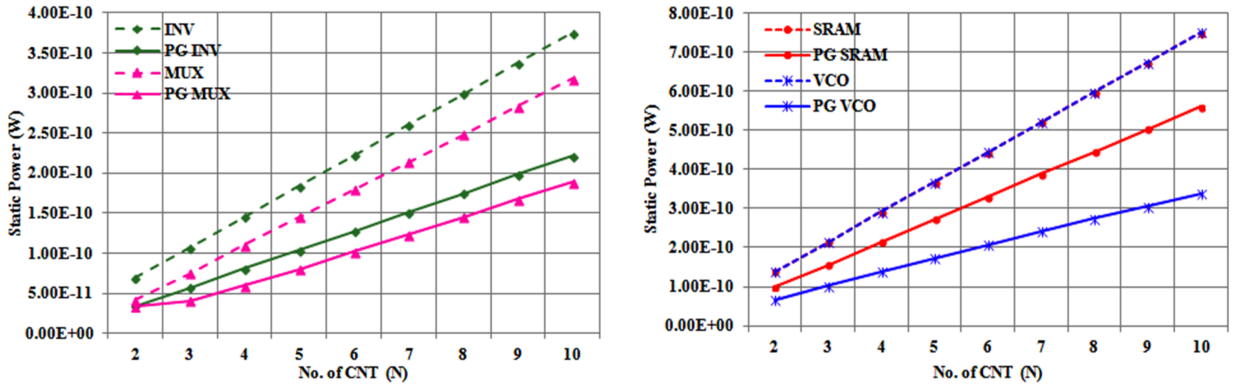

FIGURE 11. Effect of N on static power.

N	Inverter	Power gated Inverter	MUX	Power gated MUX	SRAM	Power gated SRAM	VCO	Power gated VCO
2	$1.21 \cdot 10^{-7}$	$7.85 \cdot 10^{-8}$	$9.07 \cdot 10^{-8}$	$6.55 \cdot 10^{-8}$	$6.51 \cdot 10^{-6}$	$4.47 \cdot 10^{-6}$	$1.34 \cdot 10^{-5}$	$5.96 \cdot 10^{-6}$
3	$1.80 \cdot 10^{-7}$	$1.03 \cdot 10^{-7}$	$1.37 \cdot 10^{-7}$	$9.56 \cdot 10^{-8}$	$9.70 \cdot 10^{-6}$	$6.67 \cdot 10^{-6}$	$2.00 \cdot 10^{-5}$	$8.91 \cdot 10^{-6}$
4	$2.39 \cdot 10^{-7}$	$1.25 \cdot 10^{-7}$	$1.82 \cdot 10^{-7}$	$1.27 \cdot 10^{-7}$	$1.29 \cdot 10^{-5}$	$8.86 \cdot 10^{-6}$	$2.67 \cdot 10^{-5}$	$1.19 \cdot 10^{-5}$
5	$2.98 \cdot 10^{-7}$	$1.38 \cdot 10^{-7}$	$2.27 \cdot 10^{-7}$	$1.58 \cdot 10^{-7}$	$1.61 \cdot 10^{-5}$	$1.11 \cdot 10^{-5}$	$3.33 \cdot 10^{-5}$	$1.48 \cdot 10^{-5}$
6	$3.58 \cdot 10^{-7}$	$1.53 \cdot 10^{-7}$	$2.71 \cdot 10^{-7}$	$1.90 \cdot 10^{-7}$	$1.92 \cdot 10^{-5}$	$1.32 \cdot 10^{-5}$	$3.99 \cdot 10^{-5}$	$1.78 \cdot 10^{-5}$
7	$4.17 \cdot 10^{-7}$	$1.65 \cdot 10^{-7}$	$3.15 \cdot 10^{-7}$	$2.23 \cdot 10^{-7}$	$2.24 \cdot 10^{-5}$	$1.54 \cdot 10^{-5}$	$4.66 \cdot 10^{-5}$	$2.07 \cdot 10^{-5}$
8	$4.76 \cdot 10^{-7}$	$1.65 \cdot 10^{-7}$	$3.57 \cdot 10^{-7}$	$2.54 \cdot 10^{-7}$	$2.56 \cdot 10^{-5}$	$1.76 \cdot 10^{-5}$	$5.32 \cdot 10^{-5}$	$2.37 \cdot 10^{-5}$
9	$5.35 \cdot 10^{-7}$	$1.85 \cdot 10^{-7}$	$4.04 \cdot 10^{-7}$	$2.86 \cdot 10^{-7}$	$2.88 \cdot 10^{-5}$	$1.98 \cdot 10^{-5}$	$5.99 \cdot 10^{-5}$	$2.67 \cdot 10^{-5}$
10	$5.95 \cdot 10^{-7}$	$1.96 \cdot 10^{-7}$	$4.50 \cdot 10^{-7}$	$3.16 \cdot 10^{-7}$	$3.20 \cdot 10^{-5}$	$2.20 \cdot 10^{-5}$	$6.65 \cdot 10^{-5}$	$2.96 \cdot 10^{-5}$

TABLE 4. Effect of N on dynamic power (values of dynamic power in W).

N	Inverter	Power gated Inverter	MUX	Power gated MUX	SRAM	Power gated SRAM	VCO	Power gated VCO
2	$6.93 \cdot 10^{-11}$	$3.42 \cdot 10^{-11}$	$4.16 \cdot 10^{-11}$	$3.34 \cdot 10^{-11}$	$1.39 \cdot 10^{-10}$	$9.94 \cdot 10^{-11}$	$1.38 \cdot 10^{-10}$	$6.62 \cdot 10^{-11}$
3	$1.07 \cdot 10^{-10}$	$5.72 \cdot 10^{-11}$	$7.56 \cdot 10^{-11}$	$4.06 \cdot 10^{-11}$	$2.15 \cdot 10^{-10}$	$1.57 \cdot 10^{-10}$	$2.15 \cdot 10^{-10}$	$1.03 \cdot 10^{-10}$
4	$1.46 \cdot 10^{-10}$	$8.06 \cdot 10^{-11}$	$1.10 \cdot 10^{-10}$	$5.94 \cdot 10^{-11}$	$2.92 \cdot 10^{-10}$	$2.14 \cdot 10^{-10}$	$2.91 \cdot 10^{-10}$	$1.39 \cdot 10^{-10}$
5	$1.84 \cdot 10^{-10}$	$1.04 \cdot 10^{-10}$	$1.45 \cdot 10^{-10}$	$8.03 \cdot 10^{-11}$	$3.68 \cdot 10^{-10}$	$2.72 \cdot 10^{-10}$	$3.68 \cdot 10^{-10}$	$1.74 \cdot 10^{-10}$
6	$2.22 \cdot 10^{-10}$	$1.28 \cdot 10^{-10}$	$1.79 \cdot 10^{-10}$	$1.02 \cdot 10^{-10}$	$4.45 \cdot 10^{-10}$	$3.30 \cdot 10^{-10}$	$4.44 \cdot 10^{-10}$	$2.08 \cdot 10^{-10}$
7	$2.61 \cdot 10^{-10}$	$1.51 \cdot 10^{-10}$	$2.14 \cdot 10^{-10}$	$1.23 \cdot 10^{-10}$	$5.21 \cdot 10^{-10}$	$3.88 \cdot 10^{-10}$	$5.21 \cdot 10^{-10}$	$2.42 \cdot 10^{-10}$
8	$2.99 \cdot 10^{-10}$	$1.75 \cdot 10^{-10}$	$2.49 \cdot 10^{-10}$	$1.45 \cdot 10^{-10}$	$5.98 \cdot 10^{-10}$	$4.45 \cdot 10^{-10}$	$5.98 \cdot 10^{-10}$	$2.75 \cdot 10^{-10}$
9	$3.37 \cdot 10^{-10}$	$1.98 \cdot 10^{-10}$	$2.83 \cdot 10^{-10}$	$1.67 \cdot 10^{-10}$	$6.75 \cdot 10^{-10}$	$5.03 \cdot 10^{-10}$	$6.74 \cdot 10^{-10}$	$3.07 \cdot 10^{-10}$
10	$3.76 \cdot 10^{-10}$	$2.22 \cdot 10^{-10}$	$3.18 \cdot 10^{-10}$	$1.89 \cdot 10^{-10}$	$7.51 \cdot 10^{-10}$	$5.61 \cdot 10^{-10}$	$7.51 \cdot 10^{-10}$	$3.38 \cdot 10^{-10}$

TABLE 5. Effect of N on static power (values of static power in W).

CNTFET Circuits	Dynamic Power		Static Power	
	$N = 2$	$N = 10$	$N = 2$	$N = 10$
Inverter	35	67	51	41
MUX	28	30	20	41
SRAM	31	31	28	25
VCO	56	55	52	55

Table 6. Percentage savings of power gated circuits when N is varied.

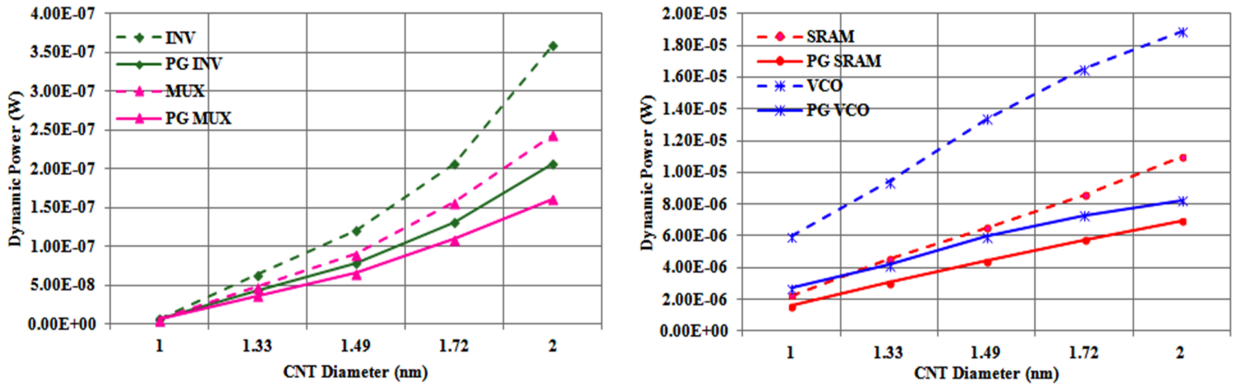

Figure 12. Effect of D_{CNT} on dynamic power.

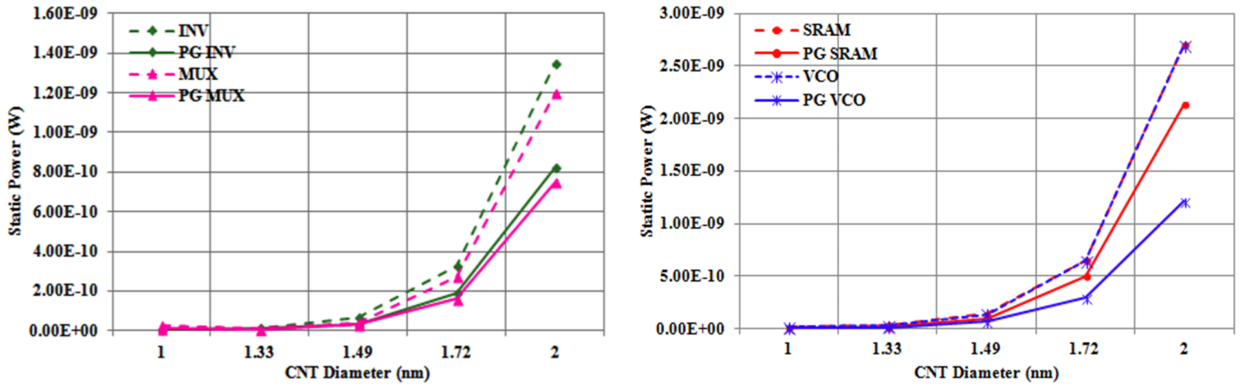

Figure 13. Effect of D_{CNT} on static power.

CNTFET Circuits	Dynamic Power		Static Power	
	$D_{\mathrm{CNT}} = 1\,\mathrm{nm}$	$D_{\mathrm{CNT}} = 2\,\mathrm{nm}$	$D_{\mathrm{CNT}} = 1\,\mathrm{nm}$	$D_{\mathrm{CNT}} = 2\,\mathrm{nm}$
Inverter	6	43	8	39
MUX	2	34	59	37
SRAM	29	36	33	21
VCO	55	56	38	55

Table 7. Percentage savings of power gated circuits when D_{CNT} is varied.

CNTFET Circuits	Dynamic Power		Static Power	
	$S = 2\,\mathrm{nm}$	$S = 20\,\mathrm{nm}$	$S = 2\,\mathrm{nm}$	$S = 20\,\mathrm{nm}$
Inverter	21	35	51	51
MUX	21	28	20	20
SRAM	28	31	41	28
VCO	53	56	53	52

Table 8. Percentage savings of power gated circuits when pitch is varied.

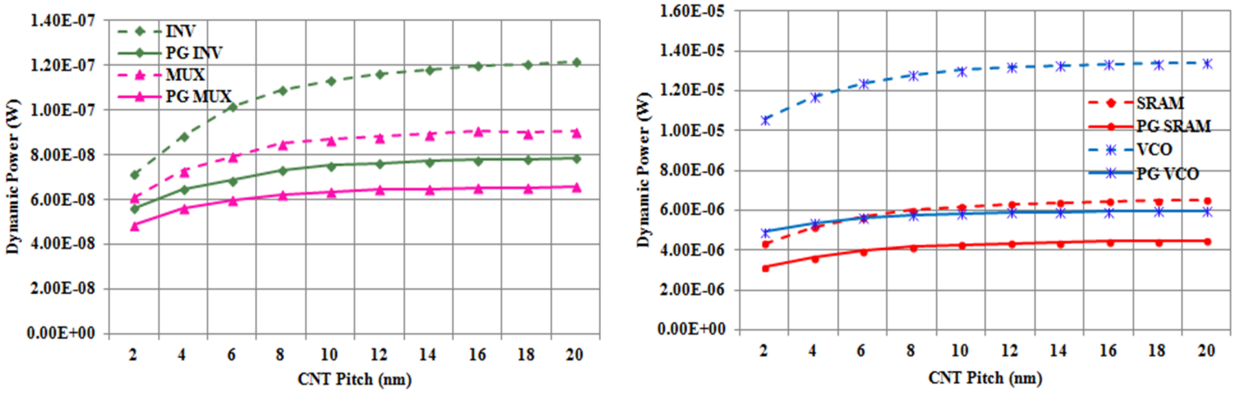

FIGURE 14. Effect of pitch on dynamic power.

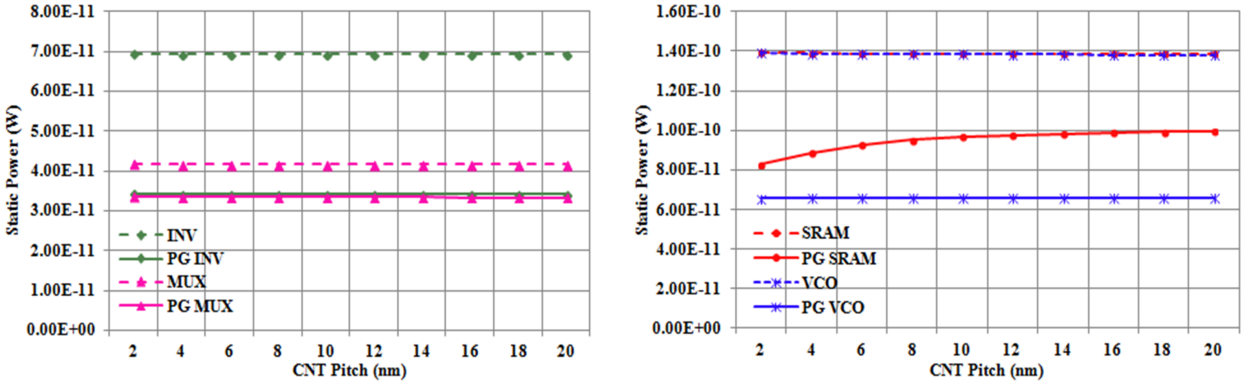

FIGURE 15. Effect of pitch on static power.

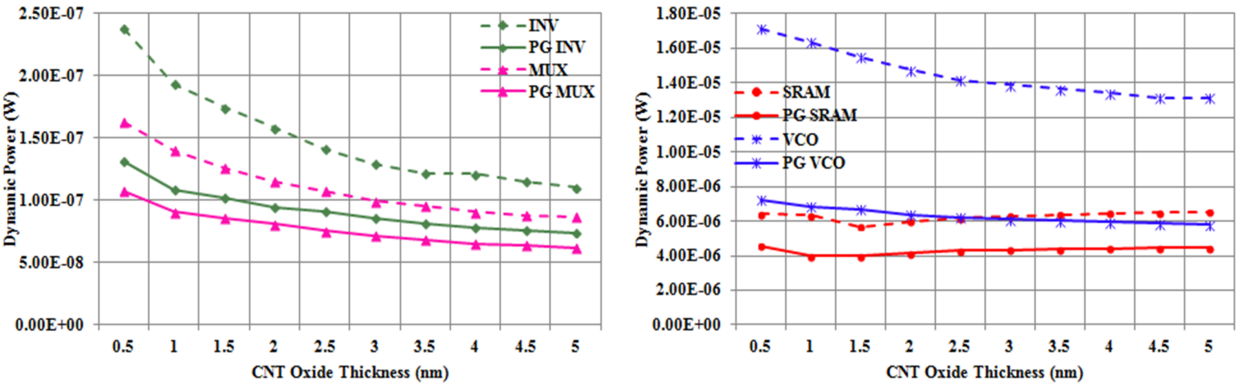

FIGURE 16. Effect of T_{ox} on dynamic power.

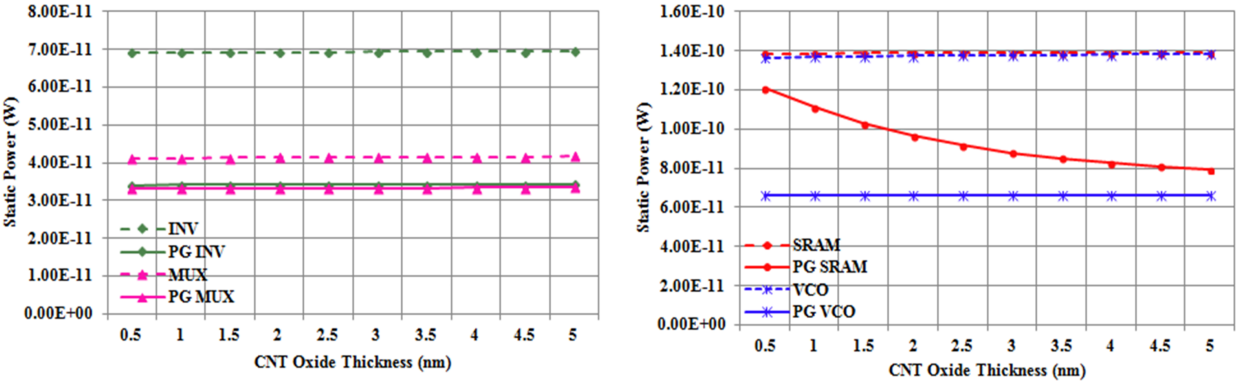

FIGURE 17. Effect of T_{ox} on static power.

CNTFET Circuits	Dynamic Power	Static Power		
	$T_{ox} = 0.5\,nm$	$T_{ox} = 5\,nm$	$T_{ox} = 0.5\,nm$	$T_{ox} = 5\,nm$
Inverter	45	33	51	51
MUX	34	29	19	20
SRAM	29	31	13	43
VCO	58	56	51	52

Table 9. Percentage savings of power gated circuits when T_{ox} is varied.

4.1. Impact of the number of carbon nanotubes (N)

In the CNTFET, the number of tubes is the important design parameter for changing the current and resistance. To provide a competitive performance over the MOSFET, a single nanotube transistor is not enough. In order to guarantee a sufficient current supply, the number of nanotubes has to be increased. The CNTFET on-current is approximately expressed as

$$I_{CNFET} = N g_{CNT}(V_{DD} - V'_{SS} - V_{th,CNT}), \qquad (4)$$

where N is the number of nanotubes per device, g_{CNT} is the transconductance per nanotube, $V_{th,CNT}$ is the threshold voltage, and V'_{SS} is the voltage drop between the inner and external source node [21] given by

$$V'_{SS} = \frac{I_{CNFET} L_S \rho_S}{N}, \qquad (5)$$

where L_s is the source length and ρ_s is the source resistance of a doped CNT. From Equation (4) and Equation (5) the CNTFET current expression can be rewritten as

$$I_{CNFET} = \frac{N g_{CNT}(V_{SS} - V_{th,CNT})}{1 + g_{CNT} L_S \rho_S}. \qquad (6)$$

Equation (6) reveals that, on the one hand, by increasing the carbon nanotubes, the device on-current can be improved. On the other hand, the power dissipation of circuits gets elevated with the increasing CNTs. Power gating structure can be used to minimize the power dissipation. Figures 10 and 11 makes it clear that the power dissipation of gated circuits is lesser, compared to conventional circuits. Tables 4 and 5 present the dynamic and static power dissipation respectively, when the number of carbon nanotubes is changed. Table 6 shows that when the number of tubes is changed from 2 to 10, dynamic power reduction of power gated circuits range from 28 % to 67 % and standby power reduction of about 20 % to 55 % is achieved compared to ungated conventional circuits.

4.2. Impact of carbon nanotube diameter (D_{CNT})

The CNTFET diameter is given by

$$D_{CNT} = \frac{a\sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi}, \qquad (7)$$

where $a = 2.49\,Å$ is the lattice constant and (n_1, n_2) is the chirality of the tube [21, 22]. The electrical behaviour and performance of the CNTFET directly depends on the CNT diameter. The on-current in a CNTFET is affected proportionally by the diameter. For larger diameters, the band gap reduces while the transconductance increases, thereby improving the on-current strength. But the leakage current is increased at the same time and this problem should be handled with care, because, for a satisfactory performance, leakage should be maintained at a minimal level. The power handling ability of CNTs degrades with large diameter values [32].

An important feature of the CNTFET is that its threshold voltage can be varied by changing the CNT diameter. Equation (8) shows that the threshold voltage is inversely related to the diameter. Hence, for a large diameter, V_{th} decreases and the power dissipation will increase:

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} = \frac{0.43}{D_{CNT}\ (nm)}, \qquad (8)$$

where $V_\pi = 3.033\,eV$ is the carbon π–π bond energy and e is the unit electron charge. Figures 12 and 13 shows the impact of the diameter on the dynamic and standby power respectively. As the carbon nanotube's diameter changes from 1 nm to 2 nm, the dynamic and static power minimization of power gated circuits varies from 6 % to 56 % and 8 % to 59 % respectively when compared to an ungated inverter and it is given in Table 7.

4.3. Impact of pitch (S)

Pitch is the distance between the centres of two adjoining CNTs under the same gate of the CNTFET. With the increase in the intertube spacing (i.e. pitch), the integration density is degraded. To enhance the integration density of a chip, shorter pitches are desirable. Equation (9) confirms that the pitch directly impacts the gate width of the device.

$$W_g = \max\{W_{min}, N * S\}, \qquad (9)$$

where W_g is the total gate width of the CNTFET, W_{min} is the minimum gate width and S is the pitch [21, 22]. For higher pitch values, the device on-current increases as the charge screening effects are lowered. Figure 14 and Table 8 show that the dynamic power minimization of power gated circuits varies from 21 % to 56 % as the pitch is changed from 2 nm to 20 nm.

Figure 15 reveals that the maximum standby power reduction of 53 % is achieved by power gated circuits as that of normal circuits when the pitch value changes from 2 nm to 20 nm.

4.4. Impact of oxide thickness (T_{OX})

The gate-to-channel capacitance decreases as the oxide thickness increases. But greater oxide thickness leads to a decreased driving current. In order to enhance the device performance, the oxide thickness of the CNTFETs has to be chosen with care. The effect of a varying oxide thickness on active and standby power is shown in the Figures 16 and 17 respectively. The simulation results in Table 9 reveals that when the oxide thickness varies from 0.5 nm to 5 nm, a dynamic power reduction of about 29 % to 58 % and maximum leakage power alleviation of 52 % is achieved in power gated circuits compared to conventional circuits.

5. Conclusions

In this paper, the applicability of a power gating structure to the CNTFETs is explored by analysing the performance of the CNTFET digital circuits. The influence of device design parameters like the number of carbon nanotubes, diameter, pitch and oxide thickness on the dynamic and standby power are investigated for the powergated and conventional circuits. The HSPICE simulation results and analysis has revealed that the power gated circuits minimize power to a great extent even under the device parameter and supply voltage variations. Hence, the LLCR power gating technique proposed for the MOSFET device structures can be extended to carbon nanotube structures to achieve a good power reduction in dynamic and standby modes of operation.

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